Abstract

A reconfigurable device comprises tiles and an interconnect architecture. Each of the tiles comprises a circuit. The interconnect architecture couples to the circuit of each tile and comprises switches and registers. In operation some of the switches route a signal from a first tile to a second tile along the interconnect architecture and at least two of the registers consecutively latch the signal at a time interval of no more than a repeating time period. In one embodiment of the reconfigurable device, the repeating time period comprises a clock cycle period. In another embodiment of the reconfigurable device, the repeating time period comprises a multiple of the clock cycle period.